

Application No. 10/777,921
Response to Office Action of December 4, 2006

Atty. Docket No. 042390.P9839C
TC/A.U. 2182

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-26 (Cancelled)

27. (New) An apparatus, comprising:

a memory buffer including

a memory module sub-interface to communicate with one or more memory modules,

a chipset sub-interface to communicate with a chipset, the chipset sub-interface being electrically isolated from the memory module sub-interface,

a data latch to latch data being transferred between the chipset sub-interface and the memory module sub-interface such that the chipset sub-interface and memory module sub-interface operate independently but in synchronization with each other, and

control logic to coordinate an output of data from the memory buffer in an interleaved mode with data from another memory buffer.

28. (New) The apparatus of claim 27, wherein the chipset sub-interface includes outputs to be interleaved.

Application No. 10/777,921
Response to Office Action of December 4, 2006

Atty. Docket No. 042390.P9839C
TC/A.U. 2182

29. (New) The apparatus of claim 27, wherein the control logic is to coordinate an output of data in a wired-OR interleaved mode.
30. (New) The apparatus of claim 27, wherein the control logic is to coordinate the output of the data interleaved with data from a single other memory buffer.
31. (New) The apparatus of claim 27, wherein the memory buffer further comprises a voltage supply line to receive a supply voltage that is independent of an operating voltage of the chipset.
32. (New) The apparatus of claim 27, wherein the memory buffer further comprises:
- a first voltage supply line to receive a first supply voltage that is compatible with an operating voltage of the chipset; and
 - a second voltage supply line to receive a second supply voltage that is compatible with an operating voltage of the memory modules.
33. (New) The apparatus of claim 27, wherein:
- the memory module sub-interface includes a first number of data lines to communicate with the memory modules; and
 - the chipset sub-interface includes a second number of data lines to communicate with the chipset, the second number being different than the first number.

Application No. 10/777,921
Response to Office Action of December 4, 2006

Atty. Docket No. 042390.P9839C
TC/A.U. 2182

34. (New) The apparatus of claim 33, wherein the first number is twice the second number.
35. (New) The apparatus of claim 27, wherein the memory module sub-interface comprises fixed length stub data lines to communicate with the memory modules.
36. (New) The apparatus of claim 27, wherein:
the memory module sub-interface is to operate at a first voltage;
and
the chipset sub-interface is to operate at a second voltage, the second voltage being different than the first voltage.
37. (New) The apparatus of claim 36, wherein the first voltage is between 1.2 and 1.8 volts.
38. (New) The apparatus of claim 36, wherein the second voltage is less than 1.0 volt.
39. (New) The apparatus of claim 27, wherein:
the memory module sub-interface is to operate at a first frequency; and
the chipset sub-interface is to operate at a second frequency, the second frequency being different than the first frequency.

Application No. 10/777,921
Response to Office Action of December 4, 2006

Atty. Docket No. 042390.P9839C
TC/A.U. 2182

40. (New) The apparatus of claim 39, wherein the first frequency is greater than the second frequency.
41. (New) The apparatus of claim 27, wherein the memory module sub-interface comprises a dynamic random access memory (DRAM) sub-interface to communicate with a DRAM module.
42. (New) The apparatus of claim 27, wherein the memory module sub-interface comprises a double data rate (DDR) DRAM sub-interface to communicate with a DDR DRAM module.
43. (New) The apparatus of claim 27, wherein the memory module sub-interface comprises a double data rate quad data rate (QDR) DRAM sub-interface to communicate with a QDR DRAM module.
44. (New) The apparatus of claim 27, further comprising:
a second memory buffer including
a second memory module sub-interface to communicate with one or more memory modules, and
a second chipset sub-interface to communicate with the chipset, the second chipset sub-interface being electrically isolated from the second memory module sub-interface, the second chipset sub-interface including outputs to output data in an interleaved mode with data from the memory buffer.

Application No. 10/777,921
Response to Office Action of December 4, 2006

Atty. Docket No. 042390.P9839C
TC/A.U. 2182

45. (New) An apparatus, comprising:

a memory buffer including

a memory module sub-interface to communicate with a
memory module,

a chipset sub-interface to communicate with a chipset, the
chipset sub-interface being electrically isolated from the memory module
sub-interface and including outputs to output data in an interleaved mode
with data from another memory buffer, and

a data latch to latch data being transferred between the
chipset sub-interface and the memory module sub-interface such that the
chipset sub-interface and memory module sub-interface operate
independently but in synchronization with each other.

46. (New) The apparatus of claim 45, wherein the chipset sub-interface
comprises outputs to be interleaved in a wired-OR configuration.

47. (New) An apparatus comprising:

a buffer to be disposed in an interface between a chipset and one
or more memory modules, the buffer including

a first sub-interface with one of the chipset and the memory
modules,

a second sub-interface with the other of the chipset and the
memory modules, the second sub-interface operated at a different voltage
level and at a lower frequency than the first sub-interface, and

Application No. 10/777,921
Response to Office Action of December 4, 2006

Atty. Docket No. 042390.P9839C
TC/A.U. 2182

control logic to coordinate an output of data from the buffer
in an interleaved mode with data from another buffer.

48. (New) The apparatus of claim 47, further comprising:

a second buffer to be disposed in the interface between the
chipset and one or more memory modules, the second buffer including a
second set of data outputs, the second set of data outputs being interleaved
with outputs from one of the first sub-interface and the second sub-
interface to form the multiple interleaved interface outputs.

49. (New) The apparatus of claim 47, wherein:

the first sub-interface comprises a sub-interface with the chipset;
and
the multiple interleaved buffer outputs are to output data over the
first sub-interface to the chipset.

50. (New) The apparatus of claim 47, wherein:

an operating voltage level of said first sub-interface is less than
1.0 volt; and
an operating voltage level of said second sub-interface is
between 1.2 and 1.8 volts.

51. (New) The apparatus of claim 47, wherein the first sub-interface is
operated at twice the frequency of the second sub-interface.

Application No. 10/777,921
Response to Office Action of December 4, 2006

Atty. Docket No. 042390.P9839C
TC/A.U. 2182

52. (New) The apparatus of claim 47, wherein a number of data lines in said first sub-interface is half that of a number of data lines in said second sub-interface.